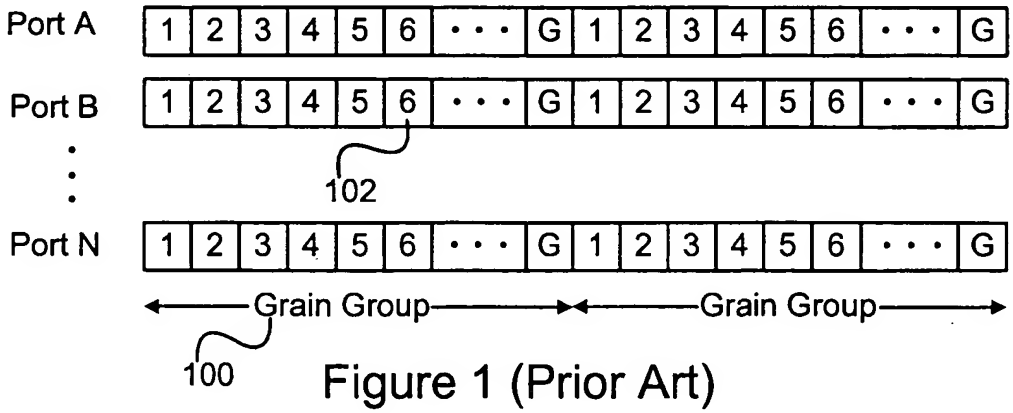


Figure 1 (Prior Art)

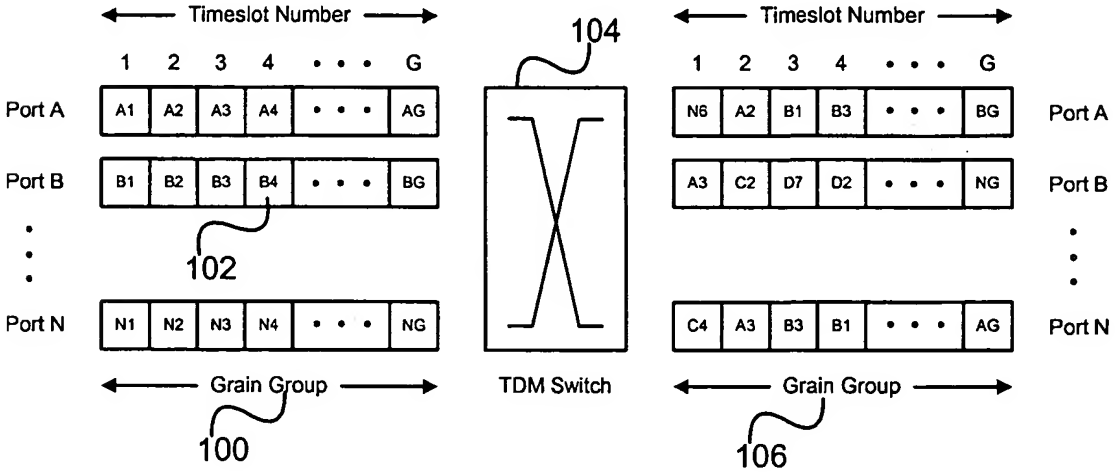
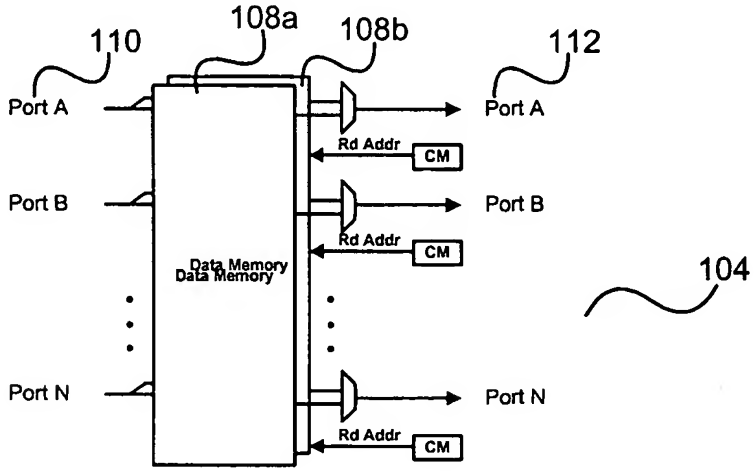


Figure 2 (Prior Art)



CM: Connection Memory

Figure 3 (Prior Art)

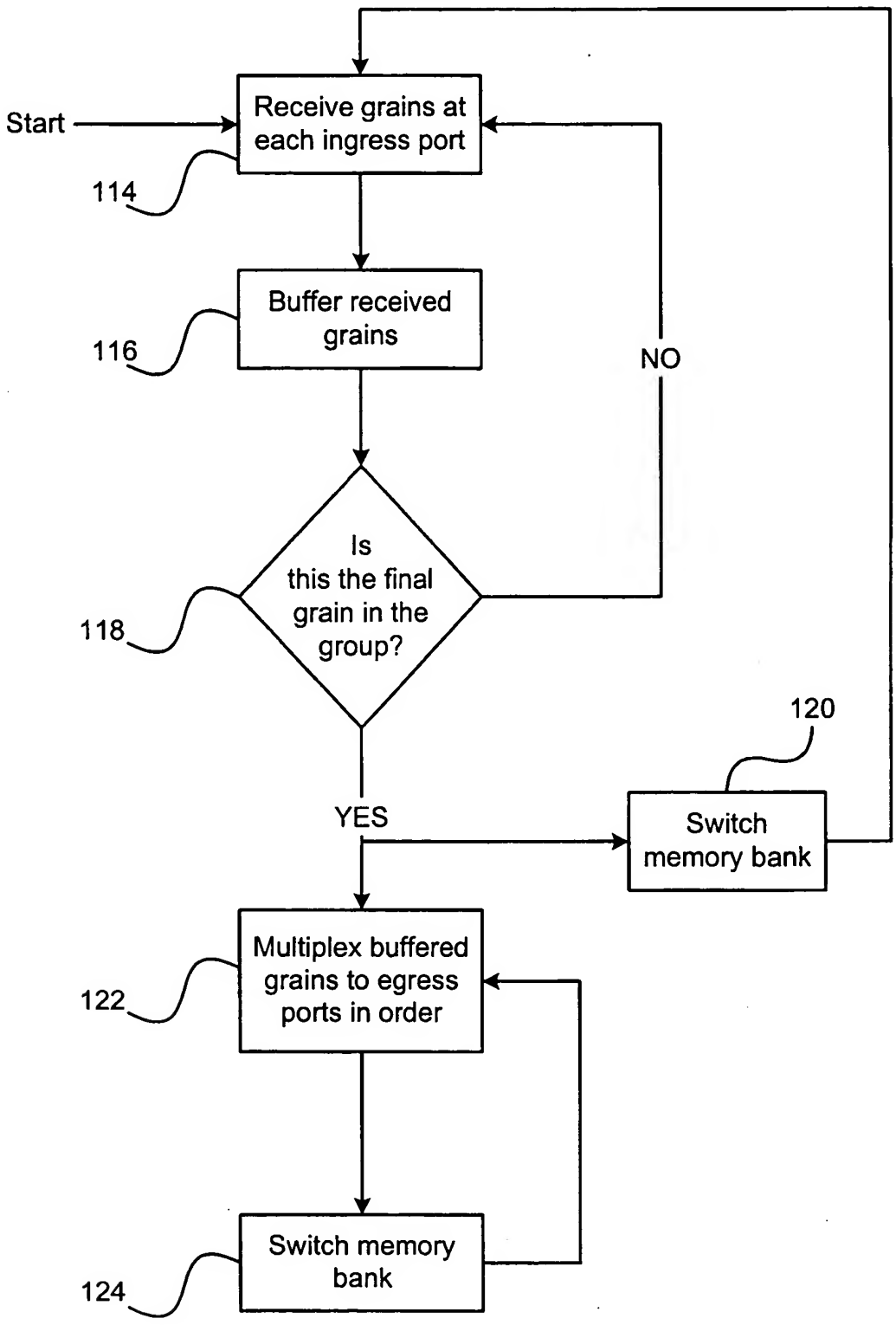


Figure 4 (Prior Art)

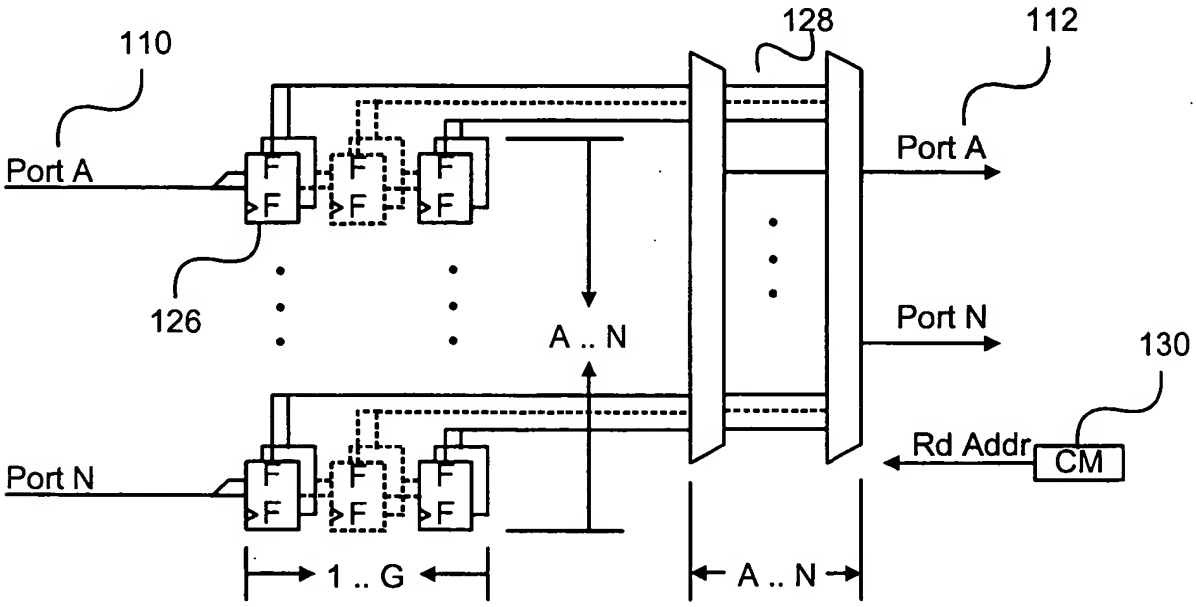


Figure 5 (Prior Art)

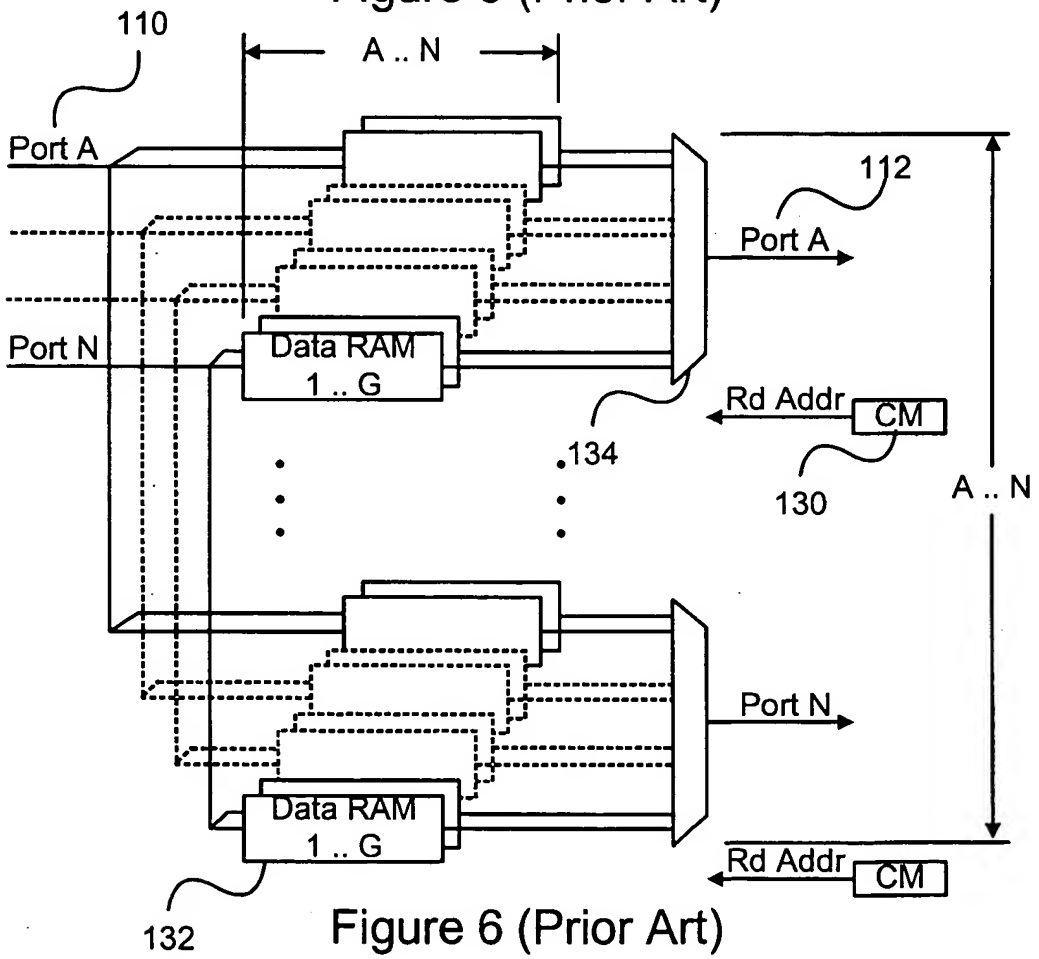
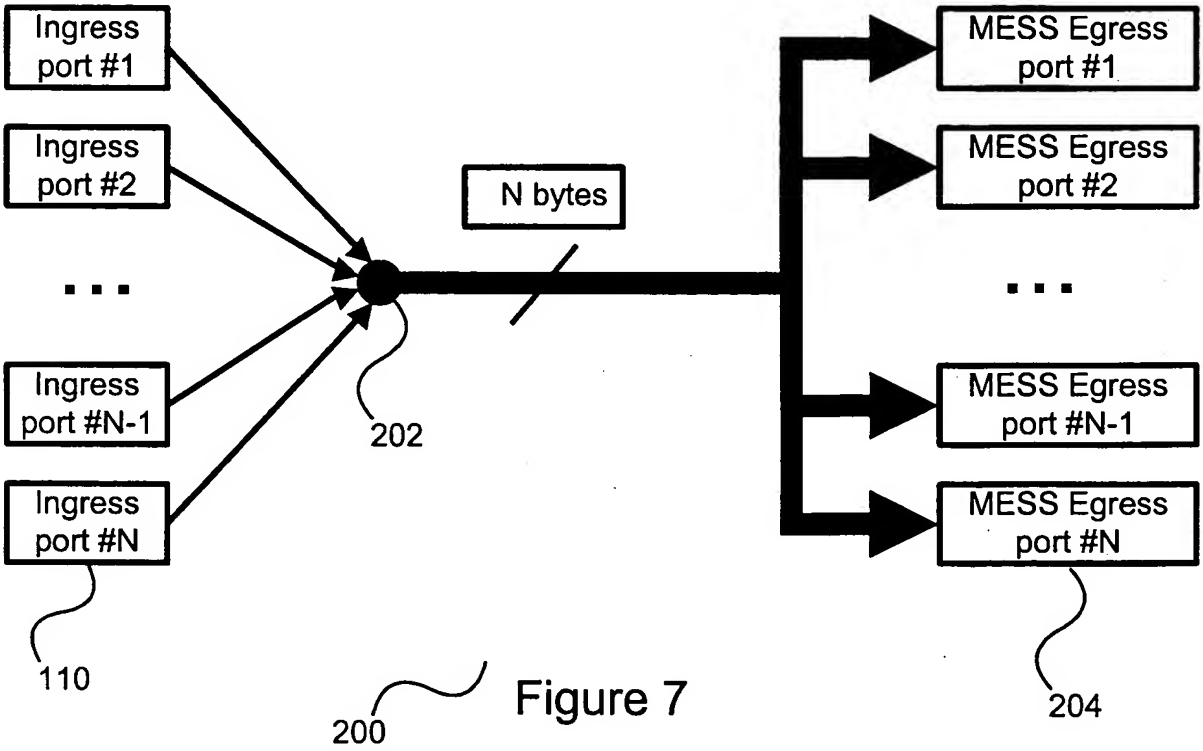


Figure 6 (Prior Art)


Ingress port #1
Ingress port #2
Ingress port #N-1
Ingress port #N
110
N bytes
202
MESS Egress port #1
MESS Egress port #2
MESS Egress port #N-1
MESS Egress port #N
204

200

Figure 7

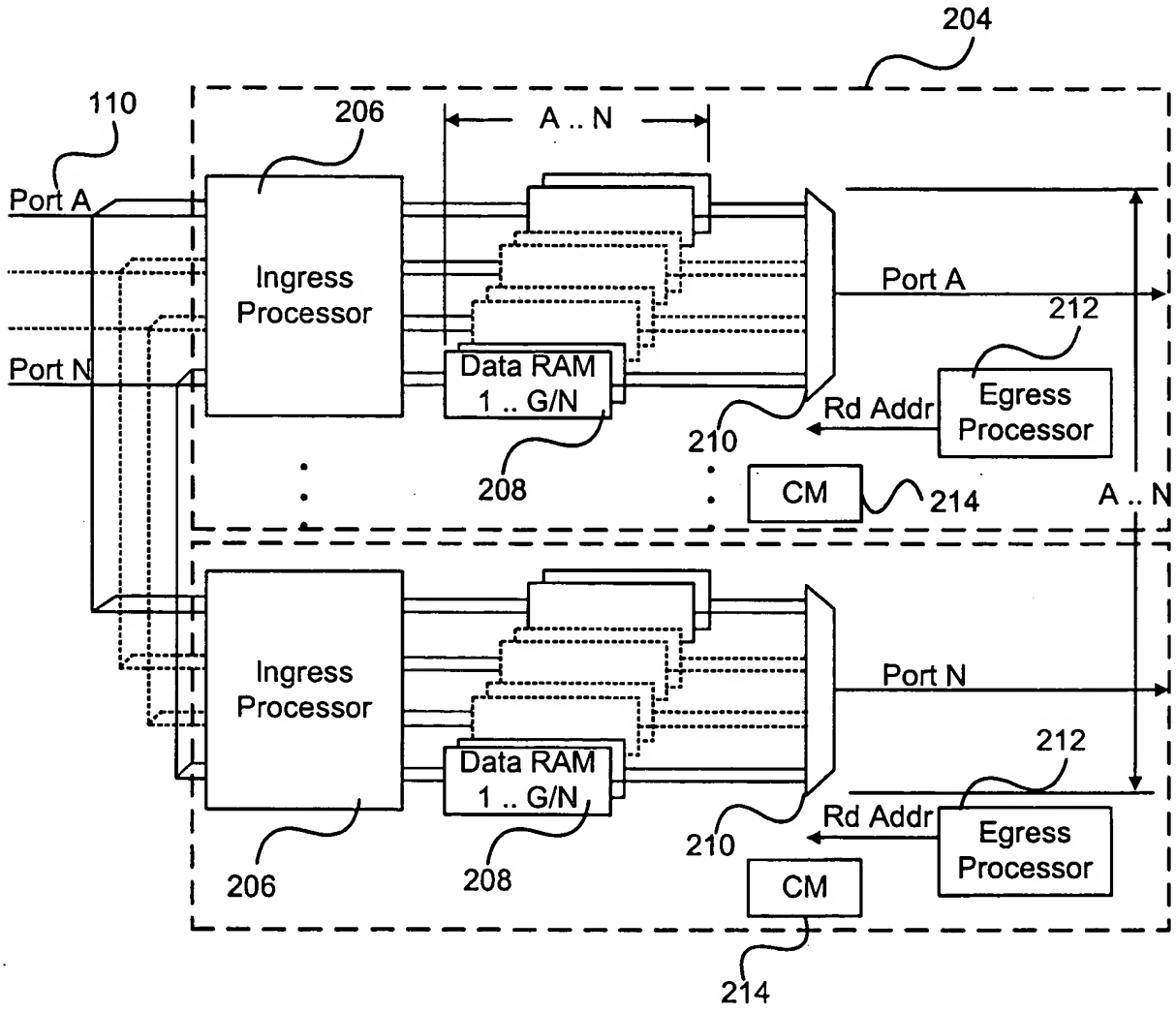

204
110
206
A .. N
Port A
Ingress Processor
Port N
Data RAM 1 .. G/N
208
210
Rd Addr
Egress Processor
212
Port A
CM
214
A .. N
Ingress Processor
Port N
Data RAM 1 .. G/N
206
208
210
Rd Addr
Egress Processor
212
CM
214

Figure 8

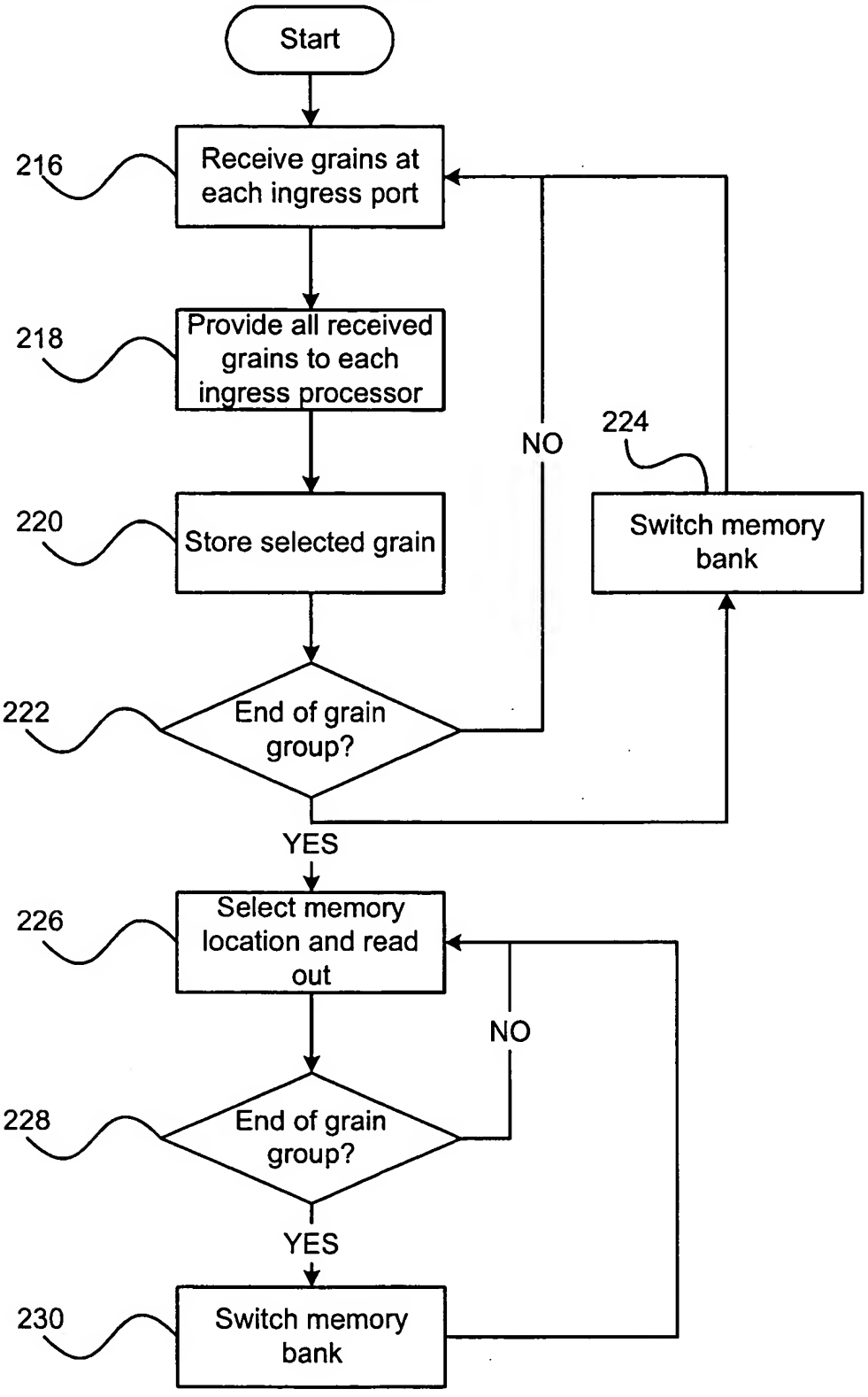

Start
216
Receive grains at each ingress port
218
Provide all received grains to each ingress processor
220
Store selected grain
222
End of grain group?
NO
224
Switch memory bank
YES
226
Select memory location and read out
NO
228
End of grain group?
YES
230
Switch memory bank

Figure 9

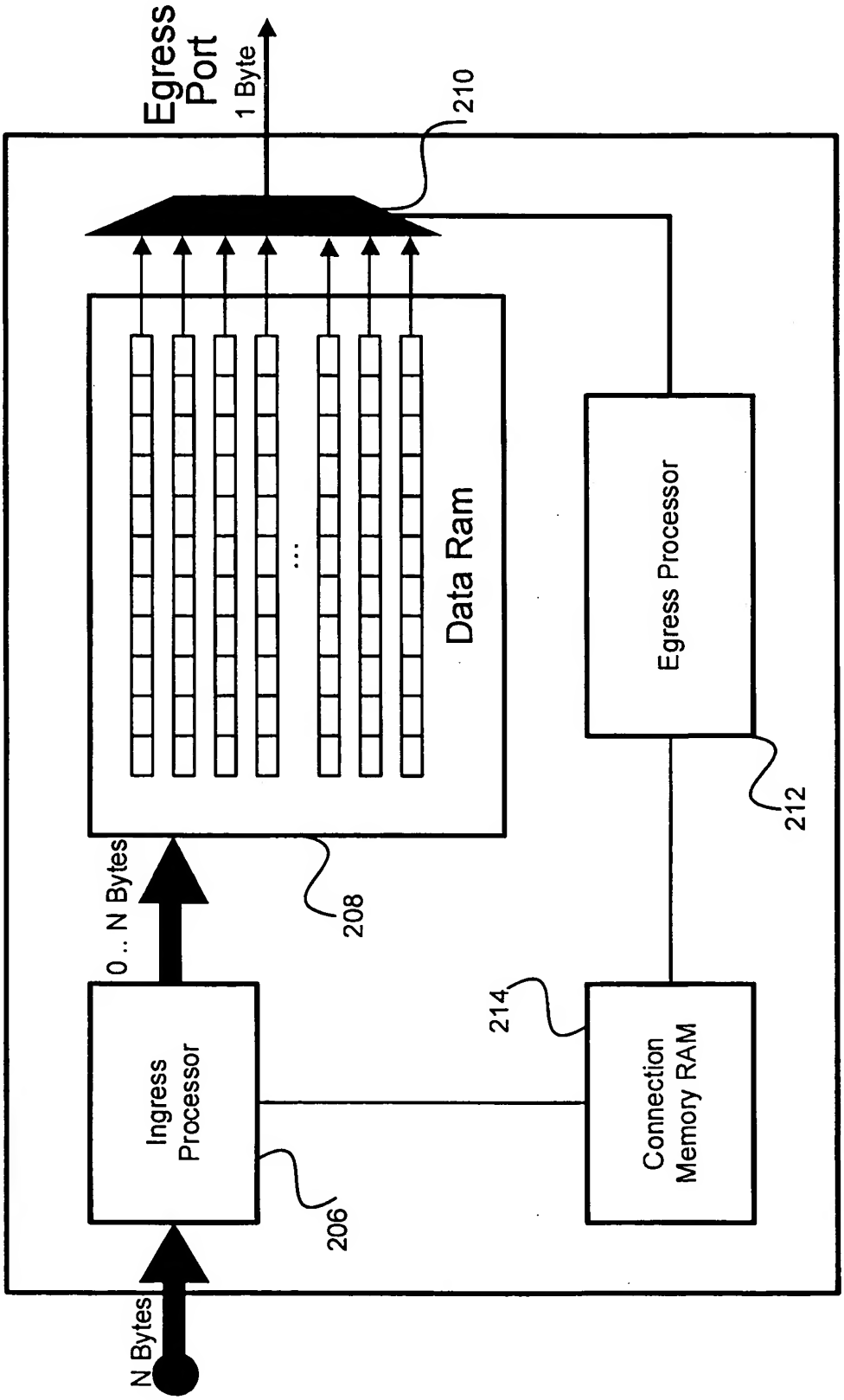

Egress Port
1 Byte
210
Data Ram
Egress Processor
212
0 .. N Bytes
208
214
Ingress Processor
Connection Memory RAM
206
N Bytes

Figure 10

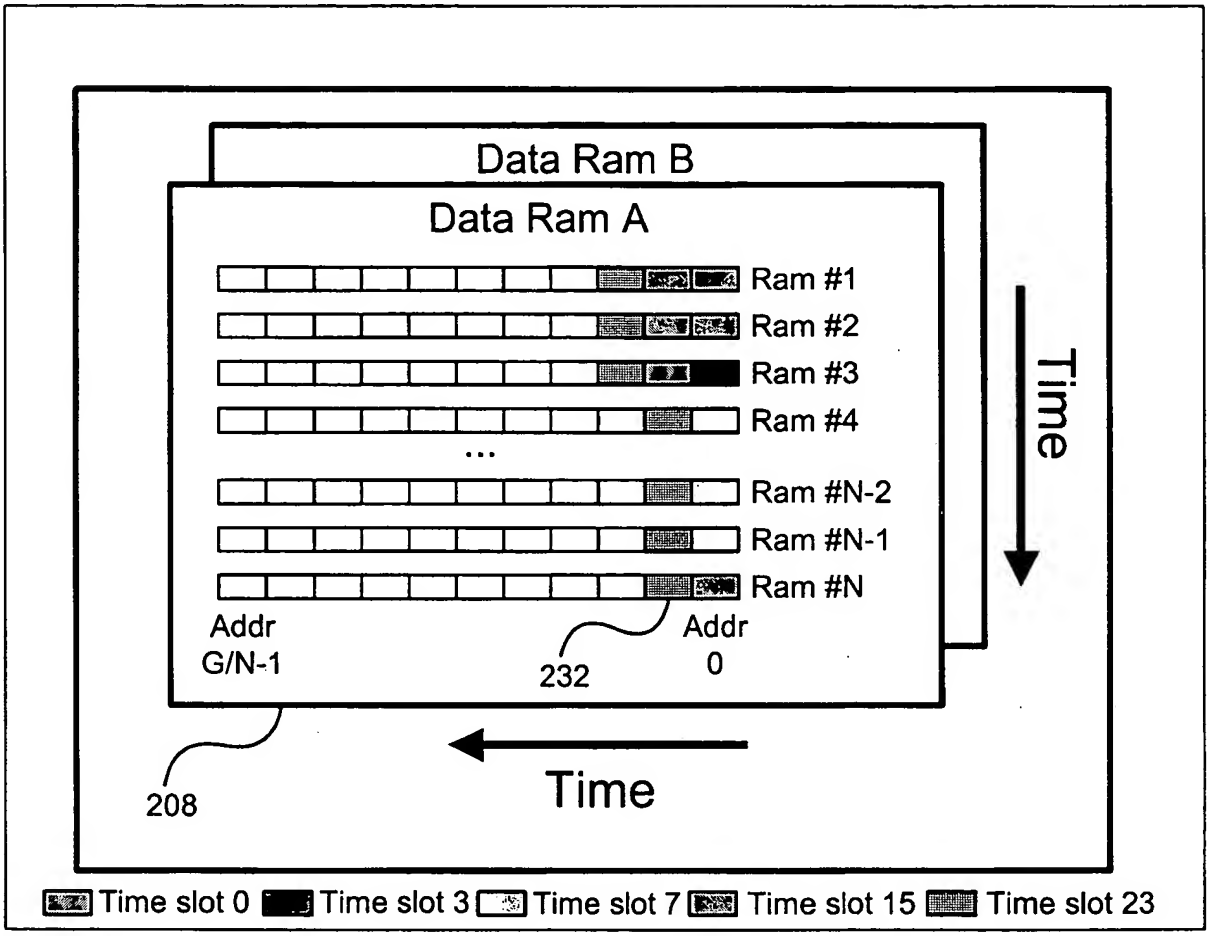

Data Ram B
Data Ram A
Ram #1
Ram #2
Ram #3
Ram #4
...
Ram #N-2
Ram #N-1
Ram #N
Addr
G/N-1
232
Addr
0
Time
208
Time
Time slot 0
Time slot 3
Time slot 7
Time slot 15
Time slot 23

Figure 11

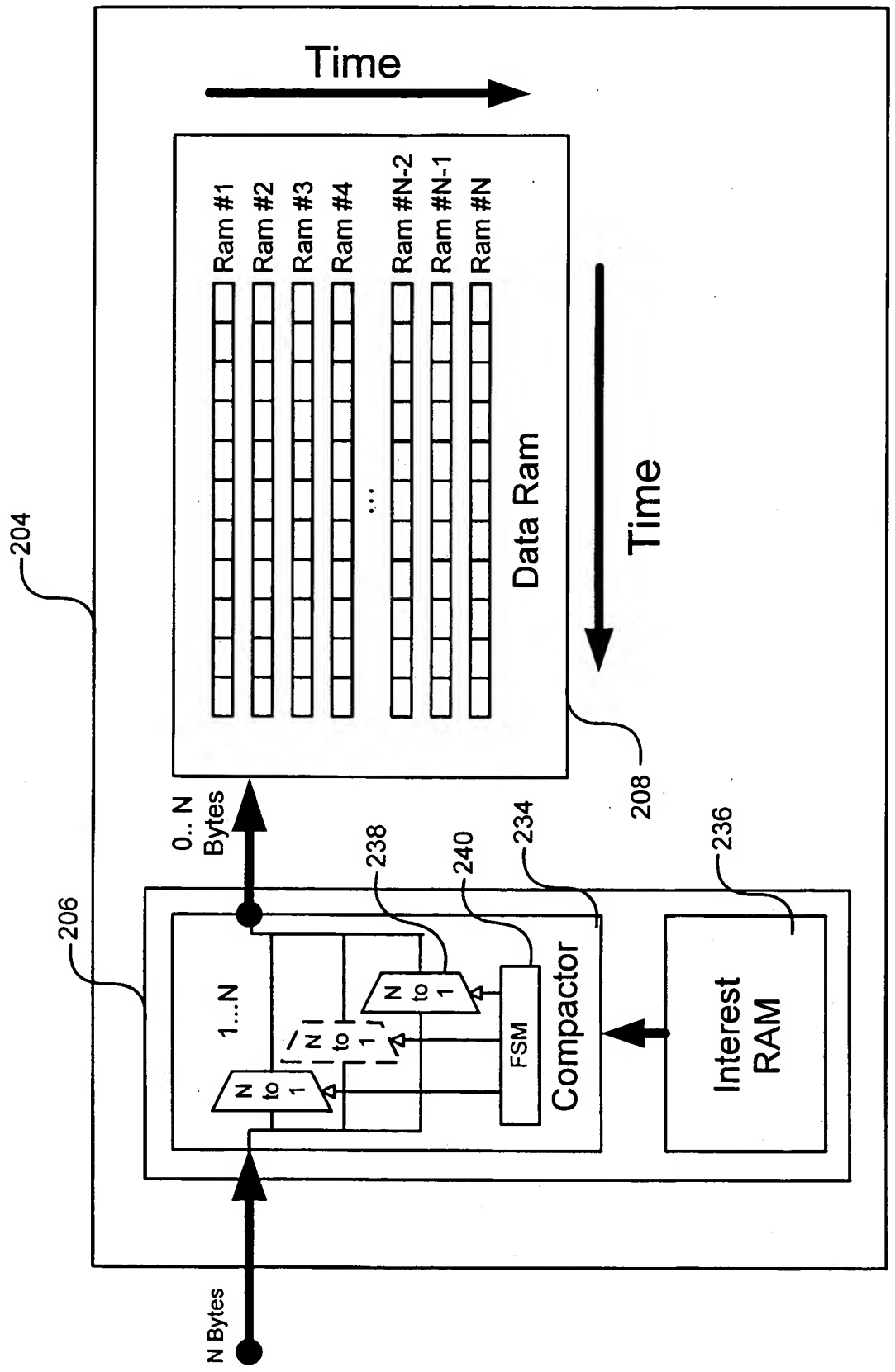

Time
Ram #1
Ram #2
Ram #3
Ram #4
Ram #N-2
Ram #N-1
Ram #N
Data Ram
Time
204
208
0.. N Bytes
238
240
234
236
206
1...N
N to 1
N to 1
FSM
Compactor
Interest RAM
N Bytes

Figure 12

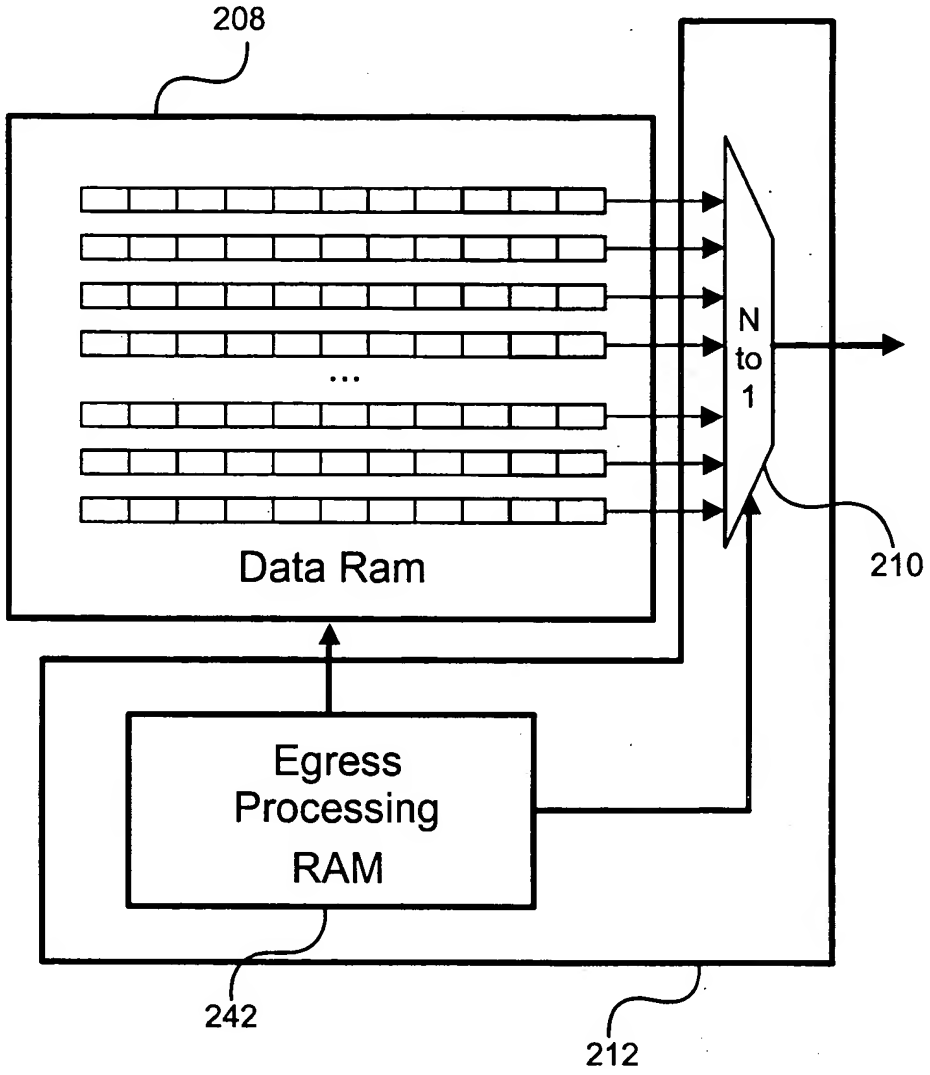


Figure 13